REMARKS

In this response to the above identified Office Action, Applicants respectfully request reconsideration in view of the above amendments and the following remarks. Applicants add new claim 22. No claims have been amended or cancelled. Accordingly, claims 1-12 and 14-22 are pending in the application.

I. Claims Rejected Under 35 U.S.C. § 101

In the outstanding action, Examiner rejects claims 17-21 under 35 U.S.C. § 101 as being directed to non-statutory subject matter. Examiner alleges that the claims are directed to a non-statutory subject matter (Office Action, Page 2) and points to "radio frequency link" in the examples for machine readable medium as the basis for the rejection. Applicants amend the specification to remove this example. Accordingly, Applicants respectfully submit that the claims are now in compliance with 35 U.S.C. §101 and respectfully requests reconsideration and withdrawal of the rejection of claims 17-21.

II. Claims Rejected Under 35 U.S.C. § 102

Claims 1-10 and 14-21 stand rejected under 35 U.S.C. § 102(b) as being anticipated by an article by Gharachorloo et al., "Two Techniques to Enhance the Performance of Memory Consistency Models (1991)" (hereinafter "Gharachorloo"). A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. MPEP § 2131. Applicants respectfully submit that each and every element in the independent claims is not set forth in the cited reference.

With regard to claim 1, it includes the limitation of "flagging a field in a reorder buffer to indicate the load instruction that uses speculative data is to be checked at retirement, the field in an entry tracking program order of the load instruction" (emphasis added). Applicants do not believe that Gharachorloo teaches these elements of the claim. Examiner cites Gharachorloo, at 2nd and 3rd full paragraphs, right col., p. 5, to teach that "[e]ach instruction, including the load instruction, is allocated a location in the reorder buffer . . . . That is, an entry (location) in the reorder buffer is flagged. This location tracks the program order of the instruction." (Office Action, p. 4.) However, the location is not, in fact, flagged to indicate that the instruction is to be checked at retirement. Although the allocation and deallocation of the location is involved in the reorder buffer's function of "allow[ing] the processor to execute [an] instruction[] past

unresolved conditional branches by providing storage for the uncommitted results," Gharachorloo, at 3rd full paragraph, lines 1-3, right col., p. 5, the cited sections do not mention any field being flagged to indicate that the instruction is to be checked at retirement. Further, a location does not constitute a discrete field in an entry, as recited in the claim. Thus, Gharachorloo does not teach each of the elements of claim 1. Accordingly, reconsideration and withdrawal of the anticipation rejection of claim 1 is requested.

With regard to independent claims 8, 14 and 17, they have similar limitations to those of claim 1 and Examiner has used similar arguments in his rejection. Thus, at least for the reasons mentioned above in regard to independent claim 1, these claims are also not anticipated by Gharachorloo. Accordingly, reconsideration and withdrawal of the anticipation rejection of claims 8, 14 and 17 based on Gharachorloo are requested.

With regard to claims 2-7, 9, 10, 15, 16 and 18-21, these claims depend from their independent claims 1, 8, 14 and 17 and incorporate the limitations thereof. Thus, at least for the reasons mentioned above in regard to these independent claims, Gharacholoo does not teach each of the elements of these claims. Applicants respectfully request the withdrawal of the rejection of claims 2-7, 9, 10, 15, 16 and 18-21 under 35 U.S.C. § 102(b) as anticipated by Gharachorloo.

III. Claims Rejected Under 35 U.S.C. § 103

Claims 11 and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Gharachorloo in view of Huck et al. "Introducing the IA-64 Architecture" (hereinafter "Huck"). To establish a *prima facie* case of obviousness: (1) there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference; (2) there must be a reasonable expectation of success; and (3) the references when combined must teach or suggest all of the claim limitations. MPEP § 2142. Applicants respectfully submit that a *prima facie* case of obviousness has not been established.

With regard to independent claim 11, it has similar limitations to those of claim 1 and Examiner has used similar arguments in his rejection. Thus, at least for the reasons mentioned above in regard to independent claim 1, claim 11 is also not anticipated by Gharachorloo. Huck does not cure the defect of lacking an entry including a field indicating that the speculative load instruction is to be checked at retirement. Applicants are unable to discern and Examiner does not identify any section of Huck that disclosures such a limitation. Therefore, the cited

references do not, singularly or combined, teach or suggest the elements of these claims. Applicants respectfully request the withdrawal of the rejection of this claim under 35 U.S.C. § 103(a) as being unpatentable over Gharachorloo in view of Huck.

Claim 12 depends from claim 11 and incorporates the limitations thereof. Thus, for at least the reasons mentioned above in regard to claim 11, Gharachorloo does not teach or suggest each of the elements of this dependent claim. Huck does not cure the deficiencies of Gharachorloo. Applicants respectfully request the withdrawal of the rejection of claim 12 under 35 U.S.C. § 103(a) as being unpatentable over Gharachorloo in view of Huck.

IV. New Claims

Applicants have added new claim 22. Support for this claim may be found in the specification at paragraphs 0018, 0023, 0026, 0028, and 0030-0033. New claim 22 includes "determining that it is unknown whether a memory address associated with a store instruction that is prior, in program order, to the load instruction conflicts with a memory address associated with the load instruction; utilizing speculative data in an execution of the load instruction by the out of order processor, if it is determined that it is unknown whether the memory address associated with the store instruction conflicts with the memory address associated with the load instruction; allocating a second entry for the load instruction in a load table, the load table being a structure for tracking only load instructions, the second entry including characteristics of an operation of the load instruction; and flagging a field in the first entry in the reorder buffer, the field to indicate that the load instruction is to be checked in relation to the load table, to confirm accuracy of the speculative data used in the execution of the load instruction, at retirement of the load instruction." Applicants are unable to discern any part of Gharachorloo or Huck that teaches or suggests these elements of the claim. Thus, Applicants submit that claim 22 is patentable over Gharachorloo and Huck.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If Examiner believes that a telephone conference would be useful in moving the application forward to allowance, Examiner is encouraged to contact the undersigned at (310) 207-3800.

Respectfully submitted,

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Dated: July 2, 2007

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I hereby certify that this paper is being transmitted online via EFS Web to the Patent and Trademark Office, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450.

Suzanne Johnston 7/2/07

Date